What is claimed is:

1. An apparatus comprising:

a delta-sigma analog-to-digital converter for converting an analog input signal, comprising:

an analog band-pass loop filter configured to filter an analog signal derived from the analog input signal, the loop filter having a center band-pass frequency; and

a quantizer configured to produce a series of digital signals by sampling the filtered analog signal from the loop filter at a sampling frequency; and

wherein the series of digital signals has a data-carrying frequency spectrum that is a mirror image of a data-carrying frequency spectrum of the analog input signal, the data-carrying spectrum of the series being located between the center band-pass frequency and zero.

2. The apparatus of claim 1, wherein the sampling frequency is f_s, the center band-pass frequency of the loop filter is f_c, and $f_s = (4/3)f_c \pm 10\%$.

3. The apparatus of claim 1, wherein the loop filter has an order of four or higher.

4. The apparatus of claim 1, further comprising a digital demodulator being coupled to receive the digital signals and configured to remove frequencies above a lower edge of the loop filter's band-pass frequency.

5. The apparatus of claim 1,

wherein the delta-sigma analog-to-digital converter further comprises:

a digital-to-analog converter configured to generate a series of analog feedback signals, each analog feed back signal corresponding to one of the digital signals; and

wherein the analog band-pass loop filter is configured to filter the analog signal derived from the analog input signal by sequentially combining the analog feedback

signals with an analog input signal.

6. The apparatus of claim 5, wherein the loop filter has an order that is higher than two.

7. The apparatus of claim 5, wherein the digital-to-analog converter is configured to generate the analog feedback signals at the sampling frequency and wherein the analog feedback signals have duty cycles of less than one.

8. The apparatus of claim 7, wherein the digital-to-analog converter is configured to generate the analog feed signals with duty cycles of less than 1/2.

9. The apparatus of claim 8, wherein the digital-to-analog converter is configured to produce the analog feedback signals in a return-to-zero format.

10. The apparatus of claim 7, wherein the digital-to-analog converter is configured to produce the analog feedback signals with duty cycles of less than about 1/3.

11. A method, comprising:

transmitting an analog input signal having a data-carrying band to a Δ-Σ ADC to convert the analog input signal into a series of digital signals having a data-carrying band, and

wherein the series of digital signals has a data-carrying frequency spectrum that is a mirror image of a data-carrying frequency spectrum of the analog input signal, the data-carrying spectrum of the series being located between the center band-pass frequency and zero.

12. The method of claim 11, further comprising:

filtering the transmitted analog input signal with a loop filter of the Δ-Σ ADC; and

sampling the filtered analog input signal to producing the digital output signals at a sampling frequency.

13. The method of claim 12, wherein the sampling frequency is f_s, a center band-pass frequency of the loop filter is f_c, and $f_s = (4/3)f_c \pm 10\%$.

14. The method of claim 12, wherein the loop filter has an order of four or higher.

15. The method of claim 11, further comprising:

filtering the digital output signals with a digital demodulator whose band pass is configured to remove frequencies higher than a lower edge of the loop filter's band pass.

16. The method of claim 11, wherein the transmitting further comprises:

performing digital-to-analog conversions of the digital output signals to sequentially produce analog feedback signals; and

producing the analog signal transmitted to the loop filter by sequentially combining the analog feedback signals with an analog input signal.

17. The method of claim 16, wherein the act of performing produces the analog feed back signals at the sampling frequency and having duty cycles of less than one.

18. The method of claim 16, wherein the act of performing produces the analog feedback signals with duty cycles of less than 1/2.